IN THE CLAIMS:

Please amend the claims as follows:

1. (Withdrawn) An overlay target comprising:
at least one trench including a series of raised lines.

2. (Withdrawn) The overlay target of claim 1, wherein said at least one trench comprises a continuous trench defining a geometric shape.

3. (Withdrawn) The overlay target of claim 1, wherein said at least one trench comprises a plurality of trenches defining said overlay target, each of said plurality of trenches includes a series of raised lines.

4. (Withdrawn) The overlay target of claim 3, wherein said plurality of trenches includes at least one continuous trench defining a geometric shape.

5. (Withdrawn) An overlay target comprising:
at least one pad area including a series of raised lines.

6. (Withdrawn) The overlay target of claim 5, wherein said at least one pad area includes a plurality of pad areas defining said overlay target, each of said plurality of pad areas includes a series of raised lines.

7. (Withdrawn) The overlay target of claim 6, further comprising at least one trench including a series of raised lines.

8. (Withdrawn) A semiconductor wafer comprising:
a semiconductor substrate; and
an overlay target comprising at least one series of raised lines.

9. (Withdrawn) The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into said semiconductor substrate.

10. (Withdrawn) The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into a material layer overlying said semiconductor substrate.

11. (Withdrawn) The semiconductor wafer of claim 8, wherein said at least one series of raised lines is disposed in at least one trench.

12. (Withdrawn) The semiconductor wafer of claim 11, wherein a plurality of trenches and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of trenches includes one of said plurality of series of raised lines.

13. (Withdrawn) The semiconductor wafer of claim 8, wherein said at least one series of raised lines is disposed in at least one pad area.

14. (Withdrawn) The semiconductor wafer of claim 13, wherein a plurality of pad areas and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of pad areas includes one of said plurality of series of raised lines.

15. (Withdrawn) The semiconductor wafer of claim 8, wherein said at least one series of raised lines comprises a first series of raised lines disposed in a pad area and a second series of raised lines disposed in a trench.

16. (Currently Amended) A method for forming an overlay target including a series of raised lines, the method comprising:
providing a substrate having an upper surface;
depositing a resist layer over the [said] substrate;

patterning the [said] resist layer to include a resist pattern defining said overlay target including a series of raised lines;

etching the [said] substrate to form the [said] overlay target including said resist pattern with the [said] series of raised lines; and

depositing a second layer of material having an upper surface thereof substantially over a portion of the upper surface of the substrate allowing the operation of a registration tool regarding the series of raised lines of the overlay target and not substantially conforming to a topography of the overlay target, said upper surface being substantially free, as deposited, of depressions in the portion thereof covering said overlay target in [said] the substrate.

17. (Previously Presented) The method of claim 16, wherein said providing a substrate comprises providing a semiconductor substrate selected from a group consisting of silicon, gallium, and sapphire substrates.

18. (Previously Presented) The method of claim 17, wherein said depositing a resist layer over said substrate comprises depositing a resist layer directly over said semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates.

19. (Previously Presented) The method of claim 16, wherein said providing a substrate includes providing a semiconductor substrate having a top surface, a bottom surface, and a material layer deposited over said top surface.

20. (Previously Presented) The method of claim 19, wherein said depositing a resist layer over said substrate comprises depositing a resist layer over said material layer and said etching said substrate to form said overlay target including a series of raised lines comprises etching said material layer.

21. (Previously Presented) The method of claim 16, wherein said etching comprises wet etching said substrate to form said overlay target including said resist pattern with said series of raised lines.